IN THE CLAIMS

Please add the following claims:

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2. An address reordering device for use in a memory system, the device comprising:

(1) a memory control block receiving dispatched addresses and sequentially performing read operations on the memory system using the dispatched addresses;

(2) a first level reorder queue storing a plurality of current addresses, each of the current addresses being equal to one of the dispatched addresses;

(3) a conflict queue storing stalled addresses, each of the stalled addresses being an address into texture memory that has its corresponding read operation postponed due to an address conflict;

(4) an in-order tag queue storing first tag information, each piece of first tag information corresponding to an address in the first level reorder queue;

(5) an out-of-order tag queue storing second tag information, each piece of second tag information corresponding to an address in the conflict queue;

(6) a conflict detection block comprising:

(6a) logic receiving a new address into texture memory, the new address being part of a sequence of addresses being received in a specific order;

(6b) logic detecting a memory conflict between the new address and any of the plurality of current addresses;

(6c) logic dispatching the new address to the memory control block if the conflict was not detected so as to make the new address into one of the dispatched addresses;

(6d) logic writing the new address into the first level reorder queue if the conflict is not detected so as to make the new address into one of the current addresses;

(6e) logic writing the new address into the conflict queue if the conflict is detected so as to make the new address into one of the stalled addresses;

(6f) logic writing new tag information corresponding to the new address into the in-order tag queue if the conflict is not detected;

(6g) logic writing the new tag information corresponding to the new address into the out-of-order tag queue if the conflict is detected; and

(6h) logic determining when the stalled addresses are dispatched to the memory control block; and

(7) logic reassembling data read from the memory system into the specific order, the reassembling being done according to the first tag information and the second tag information.

3. An address reordering method for use in a memory system, the method comprising the steps:

maintaining a list of current addresses, each of the current addresses being an address into a memory system that has been dispatched to the texture memory as part of a memory read operation that has not yet completed;

maintaining a list of stalled addresses, each of the stalled addresses being an address into the memory system that has its corresponding read operation postponed due to an address conflict;